MRAM device according to example embodiments. The memory controller **320** may provide a control signal for controlling the memory **310**.

The MRAM device according to example embodiments may be used in various types of electronic devices, e.g., mobile devices, memory cards, computers, etc.

Referring to FIG. **23**, an electronic device **2300** including a semiconductor device according to example embodiments disclosed herein may be used in, but not limited to, a computing device, a personal digital assistant (PDA), a laptop computer, a mobile computer, a web tablet, a wireless phone, a cell phone, a smart phone, a digital music player, or a wireline or wireless electronic device. The electronic device **2300** may include a controller **2310**, an input/output device **2320** such as, but not limited to, a keypad, a keyboard, a display, or a touch-screen display, a memory **2330**, and a wireless interface **2340** that are combined to each other through a bus **2350**. The controller **2310** may include, for example, at least one microprocessor, a digital signal process, a microcontroller or the like. The memory **2330** may be configured to store a command code to be used by the controller **2310** or a user data. The memory **2330** may include a semiconductor device according to example embodiments of the inventive concept. The electronic device **2300** may use a wireless interface **2340** configured to transmit data to or receive data from a wireless communication network using a RF signal. The wireless interface **2340** may include, for example, an antenna, a wireless transceiver and so on. The electronic system **2300** may be used in a communication interface protocol of a communication system, such as, but not limited to, Code Division Multiple Access (CDMA), Global System for Mobile Communications (GSM), North American Digital Communications (NADC), Extended Time Division Multiple Access (E-TDMA), Wideband CDMA (WCDMA), CDMA2000, Wi-Fi, Municipal Wi-Fi (Muni Wi-Fi), Bluetooth, Digital Enhanced Cordless Telecommunications (DECT), Wireless Universal Serial Bus (Wireless USB), Fast low-latency access with seamless handoff Orthogonal Frequency Division Multiplexing (Flash-OFDM), IEEE 802.20, General Packet Radio Service (GPRS), iBurst, Wireless Broadband (WiBro), WiMAX, WiMAX-Advanced, Universal Mobile Telecommunication Service-Time Division Duplex (UMTS-TDD), High Speed Packet Access (HSPA), Evolution Data Optimized (EVDO), Long Term Evolution-Advanced (LTE-Advanced), Multichannel Multipoint Distribution Service (MMDS), and so forth.

Referring to FIG. **24**, a memory system including a semiconductor device according to example embodiments disclosed herein will be described. The memory system **2400** may include a memory device **2410** for storing large amounts of data and a memory controller **2420**. The memory controller **2420** controls the memory device **2410** to read data stored in the memory device **2410** or to write data into the memory device **2410** in response to a read/write request of a host **2430**. The memory controller **2430** may include an address-mapping table for mapping an address provided from the host **2430** (e.g., a mobile device or a computer system) into a physical address of the memory device **2410**. The memory device **2410** may be a semiconductor device according to example embodiments disclosed herein.

The semiconductor memory devices disclosed herein may be encapsulated using various and diverse packaging techniques. For example, the semiconductor memory devices according to the aforementioned example embodiments may be encapsulated using any one of a package on package (POP) technique, a ball grid arrays (BGAs) technique, a chip scale packages (CSPs) technique, a plastic leaded chip carrier (PLCC) technique, a plastic dual in-line package (PDIP) technique, a die in waffle pack technique, a die in wafer form technique, a chip on board (COB) technique, a ceramic dual in-line package (CERDIP) technique, a plastic quad flat package (PQFP) technique, a thin quad flat package (TQFP) technique, a small outline package (SOIC) technique, a shrink small outline package (SSOP) technique, a thin small outline package (TSOP) technique, a thin quad flat package (TQFP) technique, a system in package (SIP) technique, a multi-chip package (MCP) technique, a wafer-level fabricated package (WFP) technique and a wafer-level processed stack package (WSP) technique. The package in which the semiconductor memory device according to one of the above example embodiments is mounted may further include at least one semiconductor device (e.g., a controller and/or a logic device) that controls the semiconductor memory device. Additionally, the semiconductor memory devices disclosed herein may be part of a System on a Chip (SOC).

What is claimed is:

1. A magnetoresistive random access memory device, comprising:

a first insulating interlayer on a first region and a second region of a substrate, the first insulating region comprising a flat first upper surface;

a pattern structure comprising magnetic tunnel junction (MTJ) structures and a filling layer pattern between the MTJ structures on the first insulating interlayer over the first region, the pattern structure comprising a flat second upper surface higher than the first upper surface, and the MTJ structures comprising a pillar shape;

bit lines on the pattern structure, and each of the bit lines contacting top surfaces of the MTJ structures;

a capping layer pattern on a sidewall of each of the MTJ structures and the first insulating interlayer between the MTJ structures on the first region; and

an etch-stop layer on the pattern structure between the bit lines on the first region and the first upper surface of the first insulating interlayer on the second region, a first portion of an upper surface of the etch-stop layer on the first region being higher than a second portion of the upper surface of the etch-stop layer on the second region.

2. The device of claim **1**, wherein the capping layer pattern comprises silicon nitride or silicon oxynitride.

3. The device of claim **1**, wherein the etch-stop layer is formed on the entire first upper surface of the first insulating interlayer on the second region, a sidewall of the filling layer at an interface between the first and second regions, and a portion of an upper surface of the filling layer.

4. The device of claim **1**, wherein the etch-stop layer comprises silicon nitride, silicon oxynitride or aluminum oxide.

5. The device of claim **1**, further comprising a second insulating interlayer on the etch-stop layer on the first and second regions, the second insulating interlayer filling gaps between the bit lines.

6. The device of claim **1**, wherein the magnetoresistive random access memory device is part of a smartphone.

7. The device of claim **6**, the smartphone comprises a touch-screen display.

8. The device of claim **1**, further comprising a plurality of contact plugs, the contact plugs extending through the first insulating interlayer, wherein the contact plugs are electrically connected to the MTJ structures and the first region of the substrate.